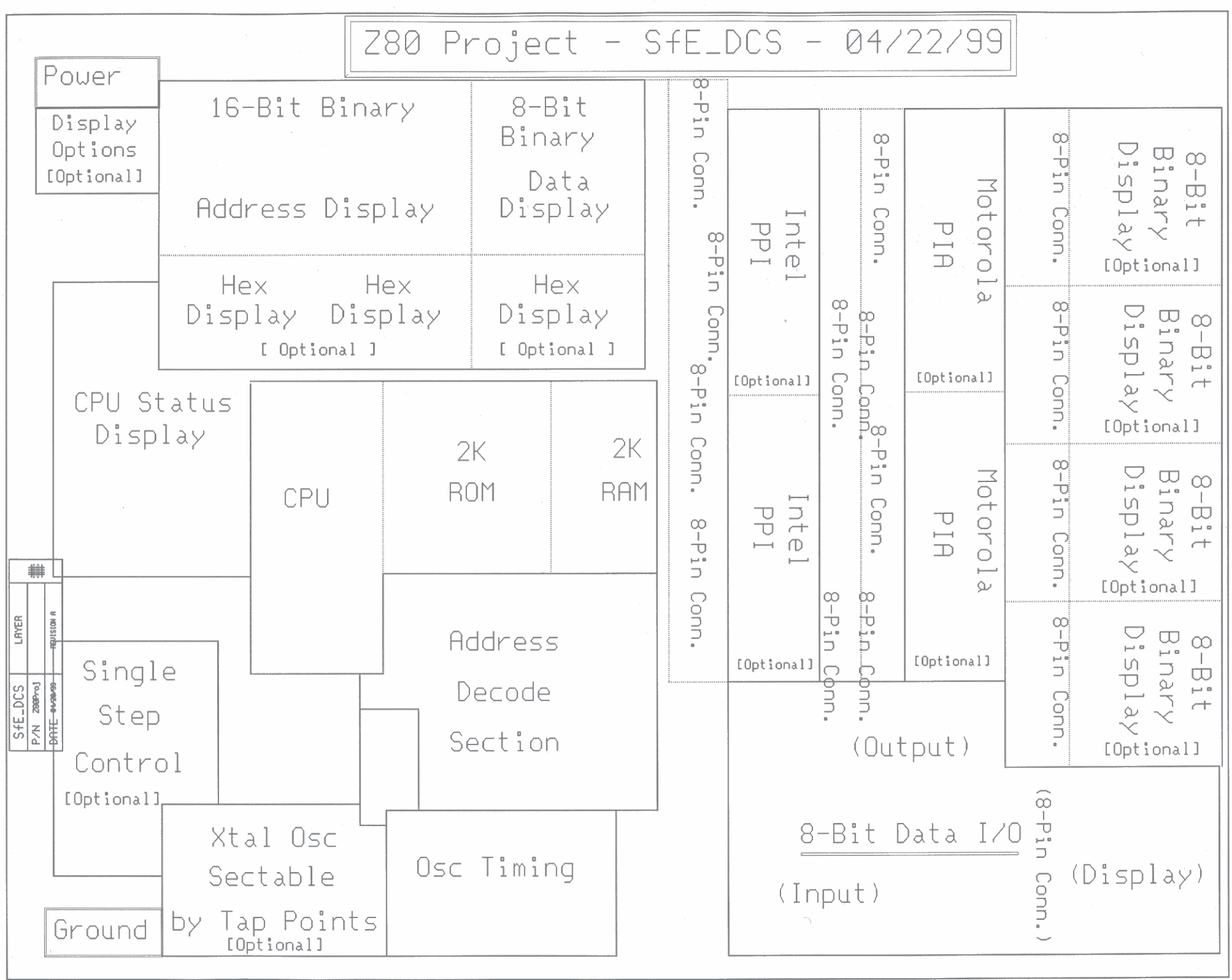
Z80 Project - SfE_DCS - 04/22/99
Power
Display Options [Optional]
16-Bit Binary Address Display
8-Bit Binary Data Display
Hex Display [Optional]
Hex Display [Optional]
Hex Display [Optional]
CPU Status Display
CPU
2K ROM
2K RAM
Address Decode Section
Single Step Control [Optional]
Xtal Osc Sectable by Tap Points [Optional]
Osc Timing
Ground
SfE_DCS
LAYER
P/N 280Proj
REVISION #
DATE
8-Pin Conn.
Intel PPI [Optional]
Motorola PIA [Optional]
8-Bit Binary Display [Optional]
(Output)
8-Bit Data I/O
(Input)
(8-Pin Conn.)
(Display)